Lecture #4

Scattering (S)-Parameter Analysis

The main objective of this lecture is to teach a useful tool for enabling a student to derive analytical transfer functions for practical circuits. Problems with worked-though solutions will be given in class.

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Radio Frequency Engineering
Lecture #4 S-Parameter Analysis

S-Parameter Revision

2-port parameters are an extremely popular way of representing circuits, active devices and passive components

A, H, Y, & Z-parameters are used extensively for low frequency circuits:
- Deal with voltages at nodes and currents in branches
- Need open- and short-circuit terminations to measure them

Scattering (or S)-parameters are used for RF & microwave frequencies
- Low inductance short circuits are hard to realise, and open circuits always have significant capacitance
- S-parameters deal with waves in transmission-lines (even if the transmission-line is actually a PCB track)
- Measured with matched source & load

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Lecture #4 S-Parameter Analysis

OVERVIEW

- S-Parameter revision
- Mason's non-touching loop rule
  - Stability analysis of active networks
  - Constant gain circles
  - Noise figure circles
- S-Parameter Analysis
  - Reflection topologies
  - Cascaded topologies
  - Tandem topologies
- Vector network analyser
  - VNA calibration
  - Time-domain Gating

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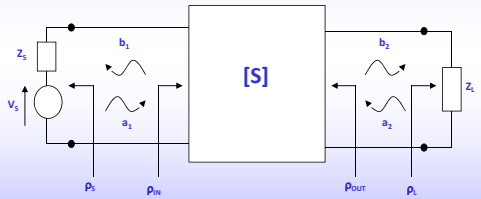
$$\text{Incident Wave, } a=\frac{V_+}{\sqrt{Zo}}=\frac{1}{2}\left(\frac{V(0)}{\sqrt{Zo}}+I(0)\sqrt{Zo}\right)\equiv+I_+\sqrt{Zo}$$

$$\text{Reflected Wave, } b=\frac{V_-}{\sqrt{Zo}}=\frac{1}{2}\left(\frac{V(0)}{\sqrt{Zo}}-I(0)\sqrt{Zo}\right)\equiv-I_-\sqrt{Zo}$$

$$\text{therefore, } V(0)=\sqrt{Zo}(a+b)\equiv(V_++V_-) \quad \text{and} \quad I(0)=\frac{(a-b)}{\sqrt{Zo}}\equiv(I_++I_-)$$



$$\text{Power Incident At Port, } P_+=|a|^2$$

$$\text{Power Reflected By Port, } P_-=|b|^2=|\rho|^2|a|^2$$

$$\text{Power Delivered to Port Termination Impedance, } P=(P_+-P_-)=\left(|a|^2-|b|^2\right)=|a|^2\left(1-|\rho|^2\right)$$

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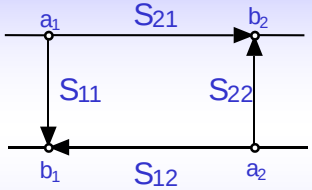
S-parameters treat the signal in terms of voltage waves (actually square root of power for a reference impedance - the "system impedance" which is normally 50 Ω)



Nodal Notation (2-nodes per port)
a1: voltage wave coming into port1
b1: voltage wave coming out from port1
a2: voltage wave going into port 2
b2: voltage wave coming out of port2

Branch Notation (signal flow paths)
S11: Reflection back from the input (INPUT MATCHING)
S21: Forward transmission from the input to the output (POWER GAIN)
S12: Reverse transmission from the output to the input (REVERSE ISOLATION)
S22: Reflection back from the output (OUTPUT MATCHING)

Power Definitions

$$\textit{Input Return Loss}, RL_{IN} = 10\log|S_{11}|^2$$

$$\left.\begin{matrix}\textit{Insertion Power Gain (Loss)}, G_I \\ \textit{Forward Transducer Power Gain (Loss)}, G_{FT}\end{matrix}\right\} = 10\log|S_{21}|^2 \quad \textit{when } Z_S = Z_L = Zo$$

$$\left.\begin{matrix}\textit{Reverse Power Isolation}, IS \\ \textit{Reverse Transducer Power Gain (Loss)}, G_{RT}\end{matrix}\right\} = 10\log|S_{12}|^2 \quad \textit{when } Z_S = Z_L = Zo$$

$$\textit{Output Return Loss}, RL_{OUT} = 10\log|S_{22}|^2$$

The value of a node = The sum of (branches entering it multiplied by the value of the node at the other end of the branch)

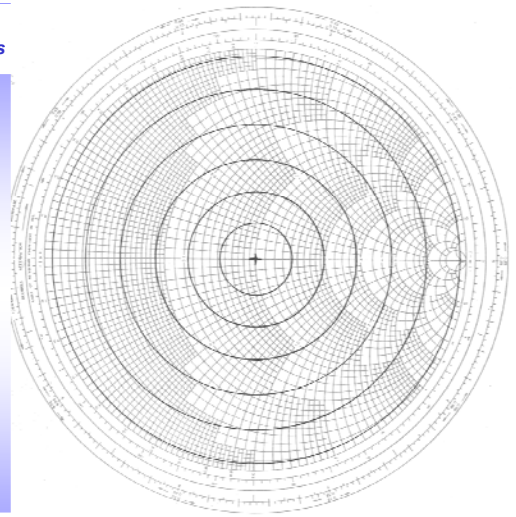
Each signal coming out of a port has two components: Some signal is transferred from the other port and some is reflected from the port:

b1=S11 . a1 + S12 . a2
b2=S21 . a1 + S22 . a2

This leads to the definitions of the S-parameters:

S11=b1/a1 (when a2=0)
S22=b2/a2 (when a1=0)
S21=b2/a1 (when a2=0)
S12=b1/a2 (when a1=0)

Impedance Smith Chart



The following features on the Impedance Smith chart are worthy of notice:

1. The (u, v) coordinate axes and the ρ(0)-plane are not explicitly marked.
2. The origin (0,0) of the chart represents an impedance-matched condition and ρ(0)=0 (i.e. $Z_T = Z_0$), for both impedance and admittance Smith charts.
3. The extreme right-hand side (1,0) of the chart represents an open circuit and ρ(0)=+1 (i.e. $Z_T = \infty$), for both impedance and admittance Smith charts.
4. The extreme left-hand side (-1,0) of the chart represents a short circuit and ρ(0)= -1 (i.e. $Z_T = 0$), for both impedance and admittance Smith charts.
5. The only straight line within the chart represents a purely resistive impedance and $|\rho(0)| \leq 1$ and θ =0° or 180° (i.e. $Z_T = R_T$).

6. The unity radius perimeter of the chart represents a purely reactive impedance and $|\rho(0)| = 1$ and θ = any value (i.e. $Z_T = jX_T$).
7. Moving along a lossless transmission line corresponds to a circular locus about the origin – in a clock-wise direction when moving away from the load and towards the generator (so that θ decreases), and in an anti-clock-wise direction when moving away from the generator and towards the load (so that θ increases).
8. Rotation of 180° produces a normalised impedance inversion, as demonstrated by the λg/4 transformer. Therefore, the Admittance Smith chart is an Impedance Smith chart that has been rotated by 180°.
9. The top half of the Impedance (Admittance) Smith chart represents positive (negative) inductive reactance (susceptance), while the bottom half represents negative (positive) capacitive reactance (susceptance).

Non-Touching Loop Rule

First identify the input and output nodes you are interested in. For example, to calculate S11 of a network you need to concentrate on a1 (input) and b1 (output)

Second, identify all the PATHS going from input to output

Third, identify any loops in the network, and note whether they touch any of your path

Fourth, apply the following equation

$$\frac{\text{output variable}}{\text{input variable}} = \frac{\sum^{all\ \ paths} P_n\left(1 - \sum_{\text{1st order loops not touching P}_n} + \sum_{\text{2nd order loops not touching P}_n} - \sum_{\text{3rd order loops not touching P}_n}\right)}{1 - \sum_{\text{1st order loops}} + \sum_{\text{2nd order loops}} - \sum_{\text{3rd order loops}}}$$

Stability Analysis

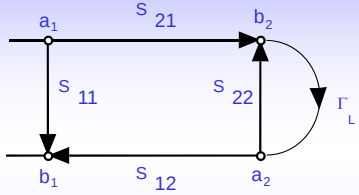
E.g. consider a transistor with some load at its output:

Input Voltage Wave Reflection Coefficient = b_1/a_1

Path 1: P1 = S11
Path 2: P2 = S21 .Γ_L . S12

Only Loop is (S22 . Γ_L), which touches P2

No 2nd or 3rd order loops



Therefore, from the rule:

$$\frac{b_1}{a_1} = \frac{S_{11}(1 - S_{22}\Gamma_L) + S_{21}\Gamma_L S_{12}(1 - 0)}{1 - S_{22}\Gamma_L} = S_{11} + \frac{S_{21}\Gamma_L S_{12}}{1 - S_{22}\Gamma_L}$$

What you connect at the OUTPUT affects the INPUT reflection coefficient, and vice versa !!!

The boundary condition for stability

$$\left| S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \right| = 1$$

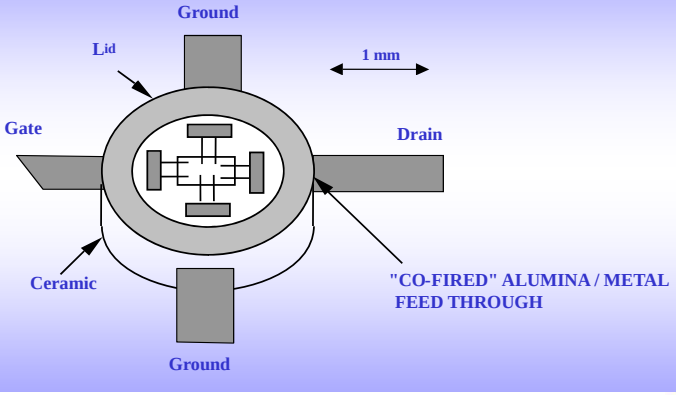
This yields a circle, whose radius is given by:

$$r_L = \frac{|S_{12}S_{21}|}{\left||\Delta|^2 - |S_{22}|^2\right|}$$

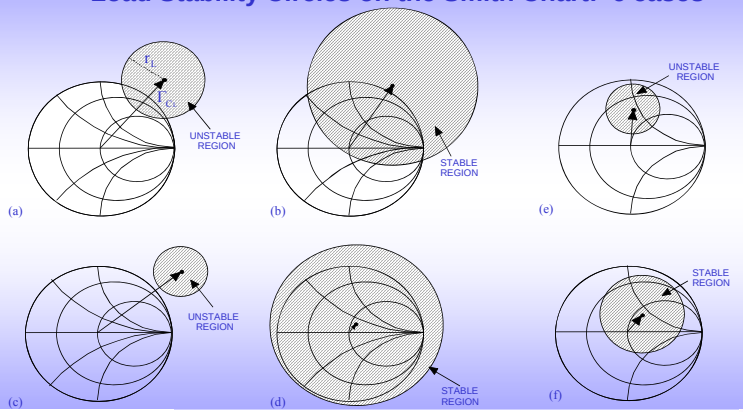
and whose centre is given by:

$$\Gamma_{C_L} = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \quad \text{where} \quad \Delta = S_{11}S_{22} - S_{12}S_{21}$$

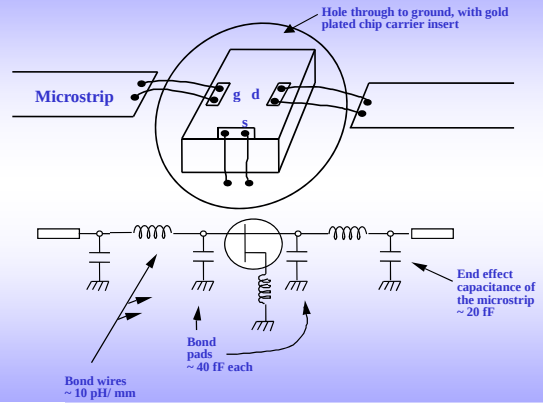
Typical ceramic package for an active FET



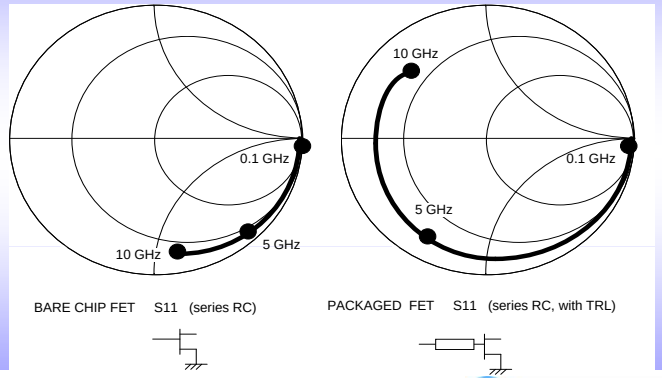
Load Stability Circles on the Smith Chart: 6 cases



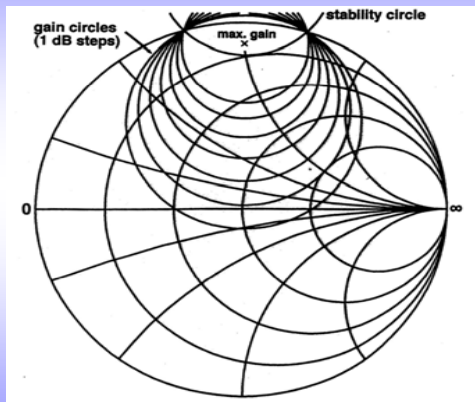
Bare-chip device and typical parasitics



The packaged FET S11 moves a lot round the chart, making wideband design difficult



Gain circles (in the Γ_L plane) at 8 GHz for a typical 300 µm FET



Z_{OUT} is in theory capacitive reactive and so the load impedance would be inductive reactive for maximum gain

Constant Gain Circles

Unilateral transducer gain:-

$$G_{TU} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)|^2} = G_S.G_0.G_L$$

$$G_S = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2} \qquad G_0 = |S_{21}|^2 \qquad G_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2}$$

• circles of constant unilateral transducer gain exist in both the G_S and G_L planes

Maximum Stable Gain

$$MSG = \left|\frac{S_{21}}{S_{12}}\right| \quad \text{for } K < 1$$

Maximum Available Gain

$$MAG = \left|\frac{S_{21}}{S_{12}}\right|\left(K - \sqrt{K^2-1}\right) \quad \text{for } K > 1$$

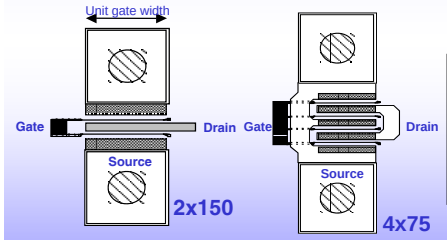
$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \qquad \Delta = S_{11}S_{22} - S_{12}S_{21}$$

RF characteristics of the FET depend on the device physics and the device GEOMETRY (i.e. its layout)

The **gate length** is the short dimension of the gate finger

The **unit gate width** is the "length" of each individual finger in the layout.

The **gate periphery** (or total gate width) is the number of fingers multiplied by the unit gate width. Gate periphery determines maximum output power



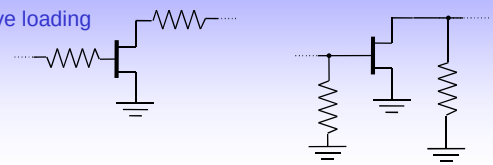
FET scaling; from 4x75 to 8x75

Most parameters scale: R/2, C x 2, gm x 2

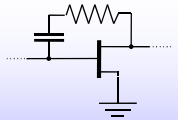
Rg depends critically on Unit gate width

Ls depends critically on physical layout

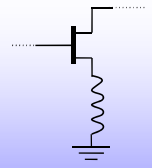
Resistive loading



Parallel feedback

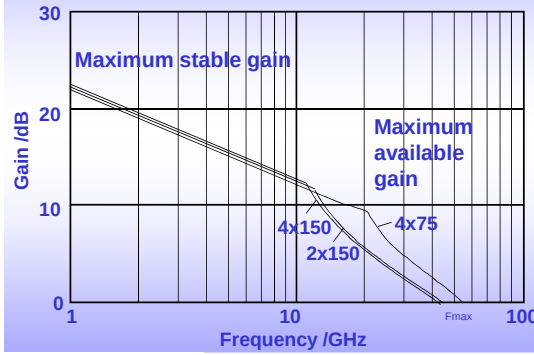


Series feedback



The Rg-Cgs pair forms a potential divider and the low-pass characteristic will effect fmax

For a given total gate width, Rg is inversely proportional to n^2 (n = number of fingers)

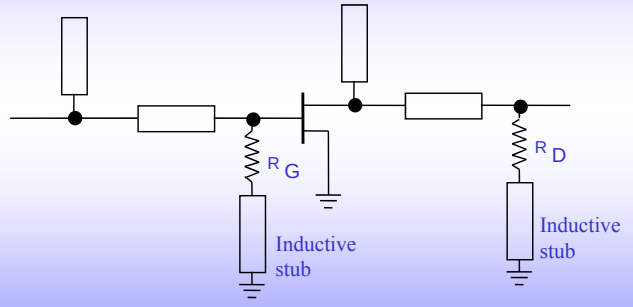


Shorter unit gate width is good!!!

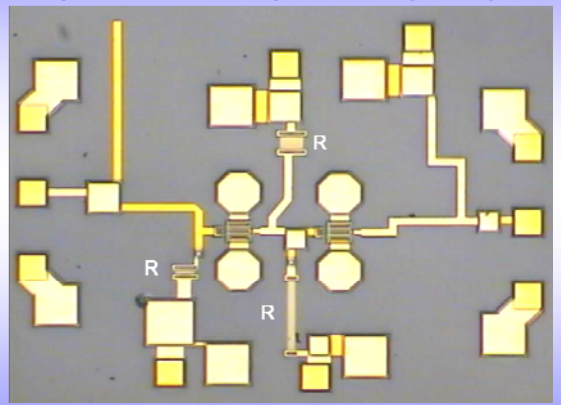
$$f_{\max} \propto \frac{n}{2}\sqrt{\frac{f_T}{2\pi C_{gd}}} =$$

$$f_{\max} \propto \frac{n\, f_T}{2\sqrt{g_{mo}}} = n \cdot constant$$

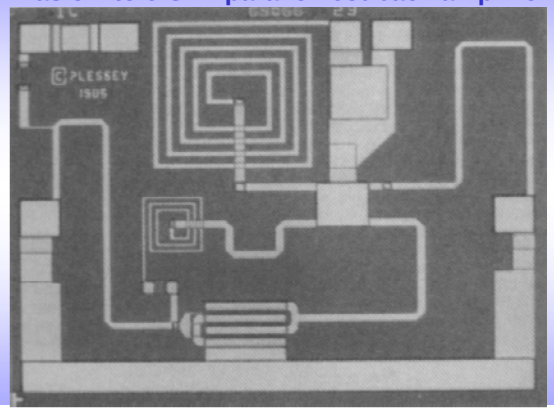
Lossy Match Amplifier (for frequency response flattening)



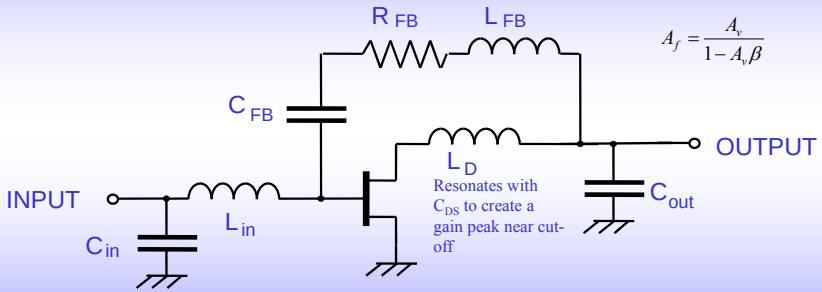
20-40 GHz pHEMT MMIC Amplifier Using Lossy Matching



Basic 1 to 6 GHz parallel feedback amplifier

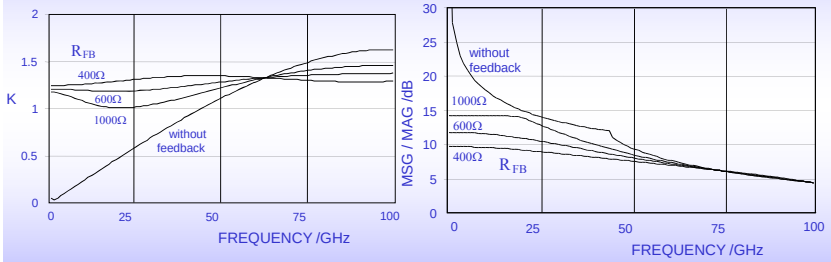


Single-Ended Parallel Feedback Amplifier

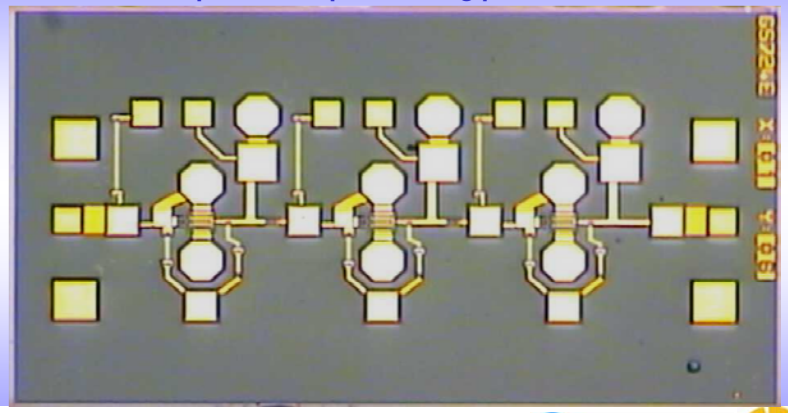


$$A_f = \frac{A_v}{1 - A_v\beta}$$

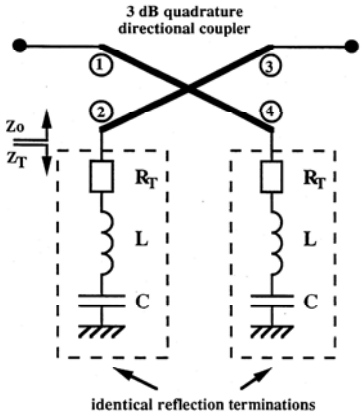
MSG/MAG and K-factor versus frequency, for a 2 x 60 mm PHEMT, with and without parallel feedback



60 GHz pHEMT amplifier using parallel feedback



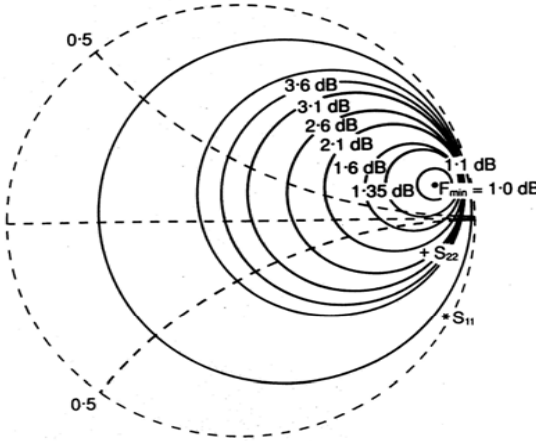
Reflection Topologies



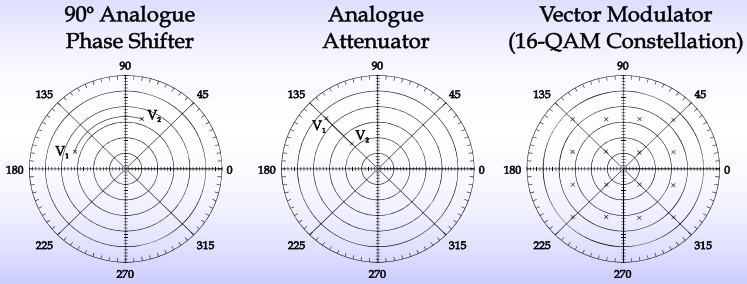
Noise Figure Circles

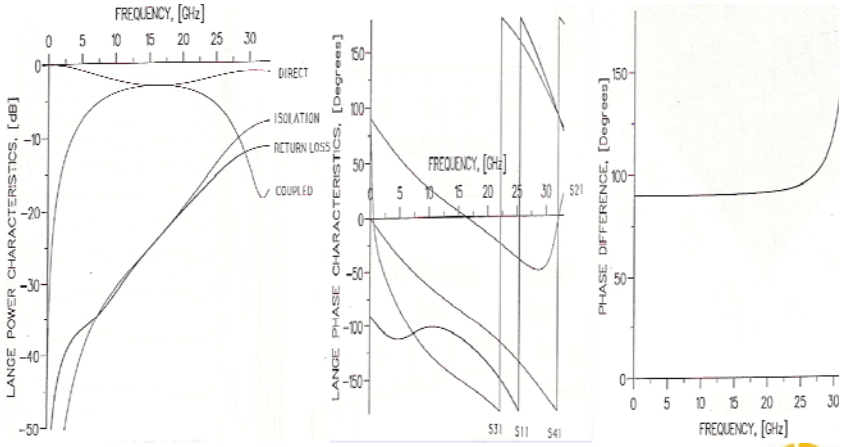
$$F = F_{\min} + 4R_n \frac{\left|\Gamma_s - \Gamma_{opt}\right|^2}{\left(1-\left|\Gamma_s\right|^2\right)\left|1+\Gamma_{opt}\right|^2}$$

minimum noise factor, F_{min}
optimum impedance, Z_{opt}
reflection coefficient, Γ_{opt}
equivalent noise resistance, R_n

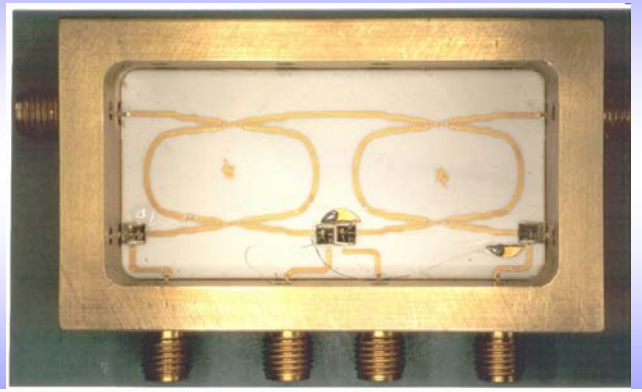


Polar plot for S21 at a single frequency



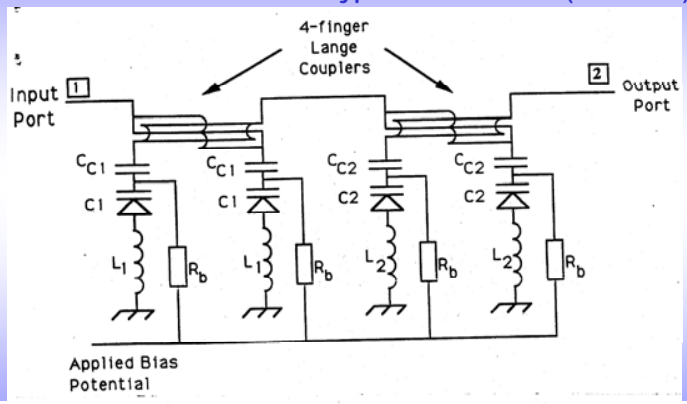


Custom-made DC to 18 GHz CMRTPS

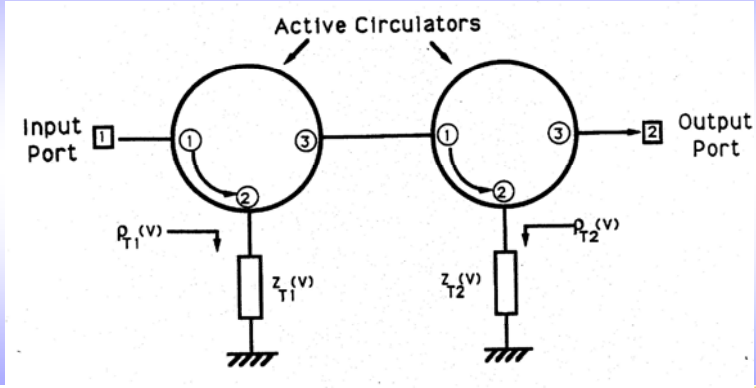


Cascaded Topologies

Cascaded-match Reflection-type Phase Shifter (CMRTPS)



Topology of the Decade Bandwidth Monolithic CMRTPS



The circulators are assumed to be symmetrical and identical. Using the 3-port steady-state S-parameters of the circulator, S_{ij} ($where\ i,j\ \varepsilon\ [1,3]$), closed form expressions for the 2-port steady-state S-parameters of the individual stages are as follows:

$$S_{11A(B)} = S_{22A(B)} = S_{11} + \frac{S_{21}S_{31}\rho_{T1(2)}}{1 - \rho_{T1(2)}S_{11}}$$

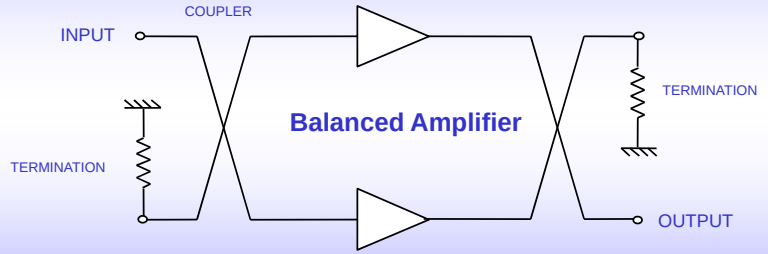
$$S_{21A(B)} = S_{31} + \frac{S_{21}^2\rho_{T1(2)}}{1 - \rho_{T1(2)}S_{11}}$$

$$S_{12A(B)} = S_{21} + \frac{S_{31}^2\rho_{T1(2)}}{1 - \rho_{T1(2)}S_{11}}$$

where, S_{mnA} = S-parameters for the first stage
S_{mnB} = S-parameters for the second stage
$m,n\ \varepsilon\ [1,2]$
ρ_{T1} = Voltage reflection coefficient of the first stage reflection termination
ρ_{T2} = Voltage reflection coefficient of the second stage reflection termination

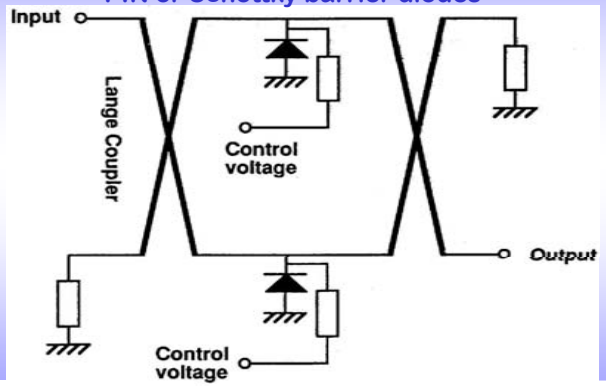
The 2-port steady-state S-parameters of the complete 2-stage CMRTPS, ($S_{11}|_{PS}$, $S_{21}|_{PS}$, $S_{12}|_{PS}$, and $S_{22}|_{PS}$), can be obtained using traditional closed form expressions for cascaded 2-port networks.

Designing for optimum gain results in non complex conjugate impedance matching and, therefore, the single-ended amplifiers will be inherently mismatched.



Tandem Topologies

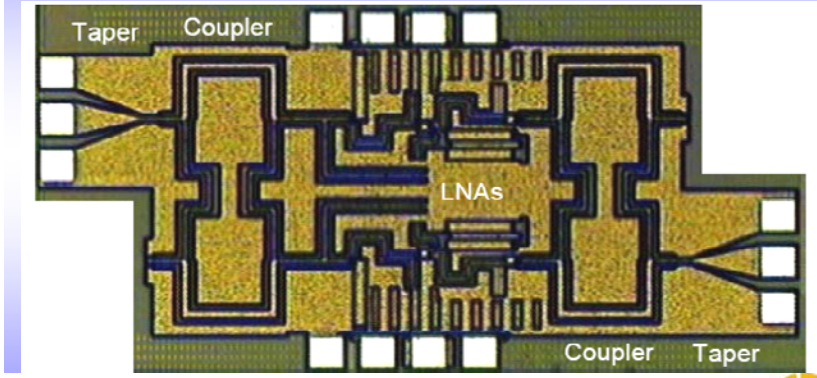
Balanced analogue attenuator employing PIN or Schottky barrier diodes



Balanced amplifier features compared with the individual single-ended amplifier

Noise figure	Single amplifier's noise figure + the coupler loss
Gain	Single amplifier's gain – 2 coupler loss
Output power	Single amplifier's + 3 dB – the coupler loss
DC power	Doubled
Reliability	Some redundancy: gain drops by 6 dB if one amplifier fails
Port matches	Excellent, easily cascaded without ripple
Stability	Excellent
Intermodulation	Third-order IMD products 6 dB lower for a given input power

60 GHz SiGe Bipolar Balanced Low-Noise Amplifiers
Brian A. Floyd, IBM (employing 90º hybrid couplers in CPW)

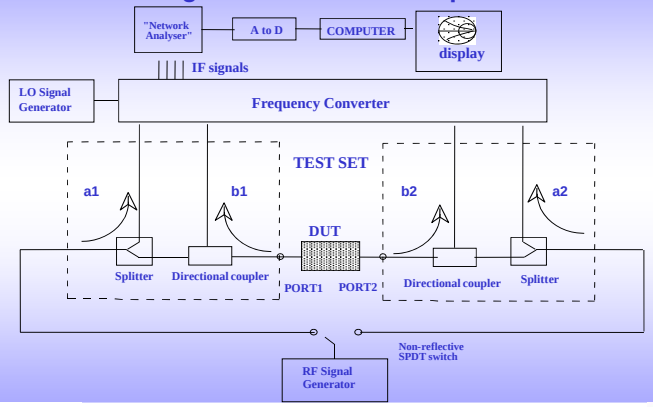


VNA Calibration

- VNAs suffer from non-ideal test-set components (e.g. reflectometer and switches) and external test components (e.g. cables, connectors and adapters)
- Unwanted transmission and reflection signals produce raw measurements (S_{ijR}) that can deviate significantly from the ideal measurements of the DUT (S_{ij})
- With a VNA, 'calibration' is the process by which the errors within the instrument (including the test-set and external test components) are compensated for
- This process is required, prior to DUT measurement, in order to quantify the effective errors and then to remove them from the raw (i.e. uncorrected) measurements

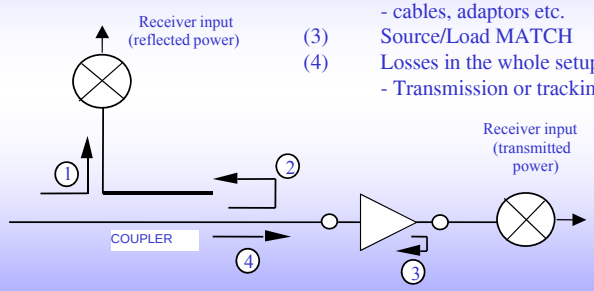
Vector Network Analyser

Simplified block diagram of a VNA with S-parameter test set



Sources of Error

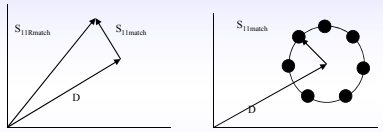
(1) DIRECTIVITY term
(2) REFLECTIONS before the DUT
- cables, adaptors etc.
(3) Source/Load MATCH
(4) Losses in the whole setup
- Transmission or tracking error



- The non-idealities of the instrument are characterised using a mathematical error correction model (represented by error adapters or boxes)
- The calibration procedure solves error coefficients by applying the raw S-parameter measurements of calibration "standards" to a set of independent linear equations
- The result of a calibration is to create two measurement reference planes, located at the 2-port DUT
- Less than perfect modelling of calibration 'standards' will result in un-corrected systematic 'residual' errors
- Residual errors can be minimised, by using high quality calibration standards, and then checked using a process known as 'verification'

- LOAD Standard:
- 'perfect' load, i.e. $S_{11match} \sim 0$ at the reference plane, determines the **Effective Directivity**, ***D***

$$S_{11Rmatch} = D + \frac{R(\sim 0)}{1 - M(\sim 0)}$$

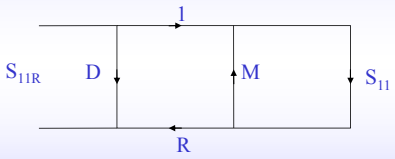


- at microwave frequencies, it is difficult to obtain a load that has an excellent impedance match over a broad bandwidth
- one alternative is to use offset loads, to create a circle of data points. The centre of the uncertainty circle is the directivity vector, while the radius of the circle is the load vector

1-Port Calibration

1-port error model

$$S_{11R} = D + \frac{R\,S_{11}}{1 - M\,S_{11}}$$

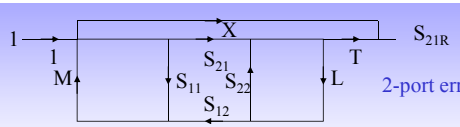


- SHORT and OPEN Standards:
- these standards are used to create a simple set of simultaneous equations, to solve for **Effective Source Match**, ***M***, and **Reflection Tracking**, ***R*** :

$$S_{11Rshort} = D + \frac{R(-1)}{1 - M(-1)} \quad and \quad S_{11Ropen} = D + \frac{R(S_{11open})}{1 - M(S_{11open})}$$

- unlike the short circuit, an open circuit is not a perfect precision standard, as there will always be a certain amount of fringe capacitance which must be accounted for!
- having evaluated D, measured $S_{11Rshort}$ & $S_{11Ropen}$ and modelled the parasitic shunt capacitance (S_{11open}) of the open, M and R can be calculated
- once this is done, S_{11} of the DUT can be 'measured'

2-Port Calibration



2-port error model

✍ LOAD Standards:

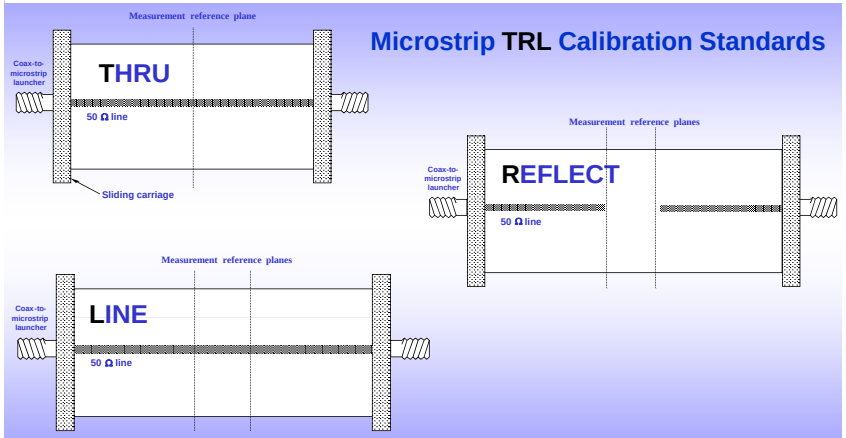
• **Isolation**, ***X***, can be measured directly, from $X = S_{21match}$, by connecting shunt load standards at both measurement reference planes

✍ THROUGH Standards:

• with the two reference planes connected together, the **Effective Load Match**, ***L***, can be measured directly from $L = S_{11}$

• once the effective load match and isolation have been measured, the **Transmission Tracking**, ***T***, can then be calculated using S_{21R}

Microstrip TRL Calibration Standards



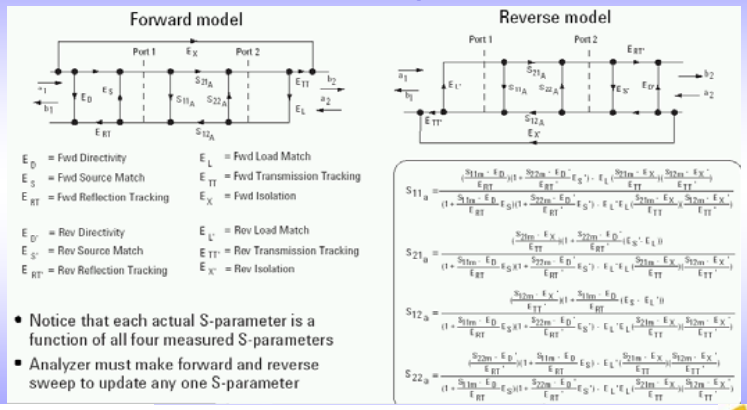
✍ VNAs have internal test-set switches to re-route the incident signals

✍ Full 2-port calibration has a 12-term error model; which corresponds to 6-terms in the forward direction (from S_{11} and S_{21}) and 6-terms in the reverse direction (from S_{22} and S_{12})

✍ Full 2-port error model equations for all four DUT S-parameters *[S]* require all forward & reverse raw measurements and all 12 error terms

✍ Each error term changes with frequency and, therefore, calibration must be performed at all the measurement frequencies

12-term error model for two-port measurements



- In practice, a complete calibration kit is required to perform this calibration procedure. This 'cal. kit' has a number of electrical reference standards and software
- For a 2-port measurement system, the calibration standards must:
  - define the primary reference planes
  - remove phase ambiguity, using open circuit and/or short circuit reflection standard(s)
  - define the reference impedance, using either delay line, matched load or attenuator impedance standard(s)
- The software should contain accurate models for the associated standards and the algorithms required to implement the chosen calibration method
- The accuracy of subsequent measurements ultimately depends on how well all the standards remain characterised

- At frequencies greater than a few hundred megahertz, DC probe needles suffer from parasitic reactance components, due to:
  - excessive series inductance of long thin needles
  - shunt fringing capacitances
- If the needles are replaced by ordinary coaxial probes that are sufficiently grounded, measurements up to a few GHz can be achieved
- The upper frequency is ultimately limited by the poor coax-to-MMIC transition
- A tapered CPW probe provides a smooth transition with low cross-talk:
  - the maximum frequency limit for coaxial-input probes is imposed by the onset of higher order modes propagating in the conventional coaxial cables and connectors
  - for operation up to 120 GHz, a coaxial cable and connector has been developed that has an outer screening conductor diameter of only 1 mm

Common Calibration Methods

Method	Calibration Standard					
	Through		Reflect	Reference Impedance		
	L=0	L≠0	$\rho_1 = \rho_2$	Line	Match	Atten.
TRL	o		o	o		
LRL		o	o	o		
TRM	o		o		o	
LRM		o	o		o	
TRA	o		o			o
LRA		o	o			o
TSD	o		ρ=-1	o		

Coaxial connector type (K, V, W are all trademarks of Anritsu):

- 3.5 mm Amphenol Precision Connector (APC3.5) is used for operation to 26.5 GHz. Unlike the 3.5 mm SMA connector, which is filled with a PTFE-type dielectric, the APC3.5 has minimal dielectric supports
- Anritsu K-connector (2.92 mm), for single-mode operation to 46 GHz, is compatible with 3.5 mm connectors
- APC2.4 can be used for measurements up to 50 GHz
- Anritsu V-connector (1.85 mm), for single-mode operation to 67 GHz, is compatible with 2.4 mm connectors
- Anritsu W-connector (1.1 mm) has a cut-off frequency of either 110 GHz or 116 GHz, depending on the coaxial dielectric used
- Agilent Technologies 1.0 mm connector is used for operation up to 120 GHz (IEEE Industry Standard Connector: insertion loss < 1 dB; repeatability ~ 40 dB)

1.0 mm Connector Design Philosophy

Connector utilizes air dielectric interface for highest accuracy and repeatability

* 1.0 mm versus W-connector is like 3.5 mm versus SMA
* The coupling diameter and thread size were chosen to maximize strength, increase durability, and provide highly repeatable interconnects

The coupling engagement of the connector is such that the outer conductors align before the center conductors engage, thus guaranteeing a damage-free connection

	1.0 mm	W* (1.1 mm)
Male Pin	precision machined	uses center conductor of .047" coax cable
Female Contact	precision machined; electrically compensated to 50-ohms	similar to 1.0 mm
Reference Plane	spec'd for flatness & finish; air dielectric	end of .047" coax cable
Pin Depth	well defined	poorly defined
Concentricity	well controlled; (0.025mm radial)	poorly controlled, limited to quality of .047" coax cable.

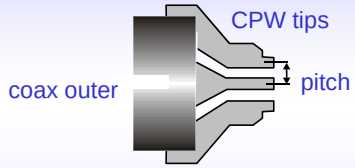
Infinity Probe™ from Cascade Microtech™

Cascade Microtech have developed tapered CPW probes and microstrip hybrid probes (Infinity) that enable measurement to be made from DC to 110 GHz with a single coaxial input.

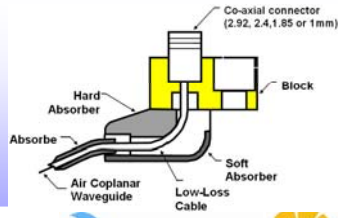
With waveguide input, 50 to 75 GHz (V-band) or 75 to 110 GHz (W-band) probes are available in both the tapered waveguide and Infinity versions.

The Infinity probes are also available for 90 to 140 GHz (F-band), 110 to 170 GHz (D-band) and 140 to 220 GHz (G-band) operation.

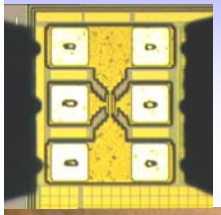
Cascade Microtech developed the *Air Coplanar*™ tipped coaxial probe:
Insertion loss of less than 1.0 dB from DC to 110 GHz
Operates at temperatures from -65 °C to +200 °C.

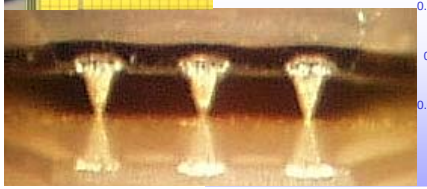


Cascade Microtech still produce the ACP probe, as it is useful for applications that require high power/bias use (above 500 mA), poor contact planarity, large pitches (above 250 μm) or temperatures above 125 ºC.

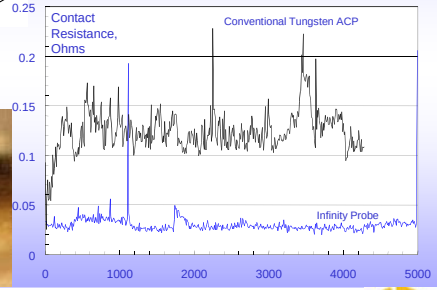


Infinity tip illustration, contact bumps in contact with wafer





- Lower contact resistance
- Extremely small contacts
- Reduced damage
- Improved isolation



- When selecting the type of microwave probe required, it is necessary to supply the vendor with the following specifications:
  - Footprint: ground-signal-ground (GSG) is the most common for MMICs, although ground-signal (GS) probes are used below 10 GHz
  - Probe tip contact pitch: commercially available from 50 µm to 1250 µm. Most common is 200 µm; 100 µm is commonly up to 120 GHz; and 75 µm above 120 GHz
  - Probe tip contact width: 40 µm and 25 µm are typical for operation up to 65 GHz and 120 GHz, respectively
  - Probe tip contact metal-plating: BeCu is optimised for GaAs chips (having gold pads) and tungsten is optimised for silicon and SiGe chips (having aluminium pads)
  - Launch angle, ϕ.

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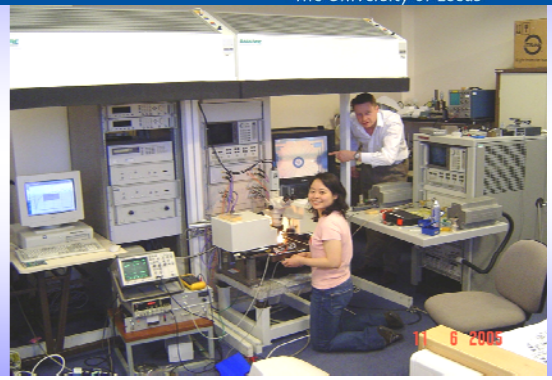
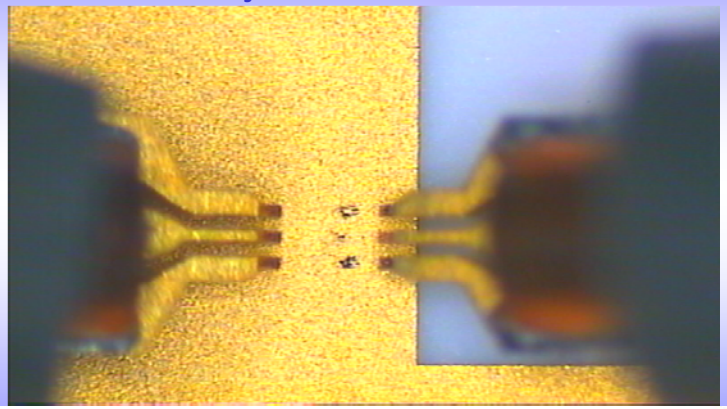


- When compared with test fixtures, commercial probe station measurements have many advantages:
  - available in a single-sweep system from DC to 120 GHz
  - much more accurate and repeatable, since they introduce smaller systematic errors
  - they have a simpler calibration procedure, which can be automated with on-wafer calibration and verification standards
  - they enable the VNA measurement reference planes to be located at the probe tips or at some distance along the MMIC's transmission line
  - they provide a fast, non-destructive means of testing the MMIC, thus allowing chip selection prior to dicing and packaging
  - overall, the microwave probe station can provide the most cost effective way of measuring MMICs when all costs are taken into account

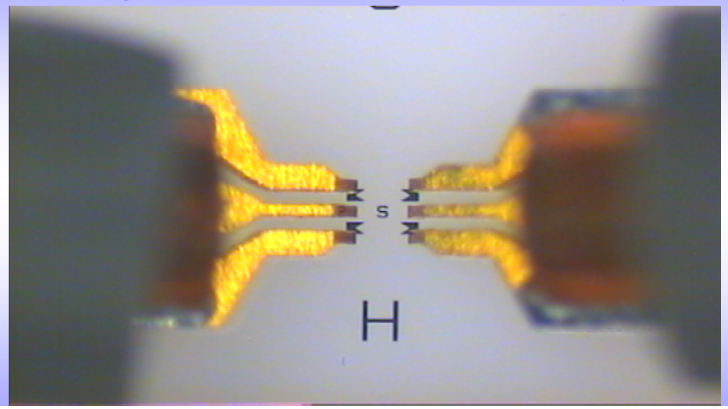
Pre-Calibration Procedure

- Through use, there are two mechanisms by which the probe tips become soiled, which will degrade mm-wave measurements:
  - particles of either Au or Al will be deposited onto the respective BeCu or W contacts
  - it is not uncommon for the probe tip contacts to overshoot the unpassivated probe pads and scratch-off some of the Si_2N_3 passivation layer surrounding the pad
- A planarity check must be made between the probes and ultra-flat surface of the wafer chuck. A contact substrate is used to ensure clear & even GSG markings in the gold
- The probe tip contacts can be cleaned of any residual gold or oxidised tungsten, by simply probing onto the exposed, un-metallised, areas of alumina
- After being inspected, cleaned, planarised & cleaned again, probes have to be aligned

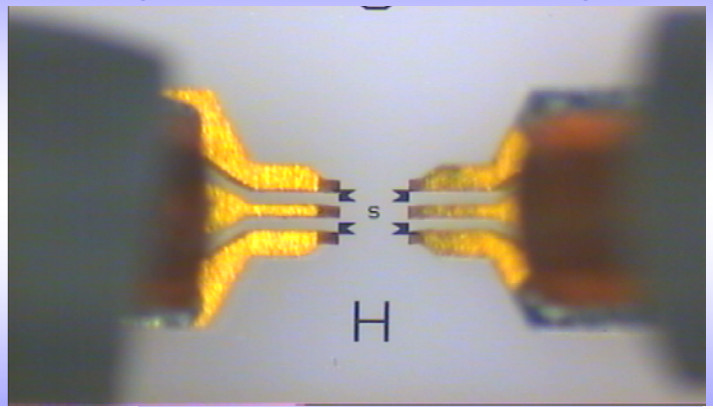
Planarity Check on Contact Substrate



Alignment Marks with Over-travel Set to 25 μm

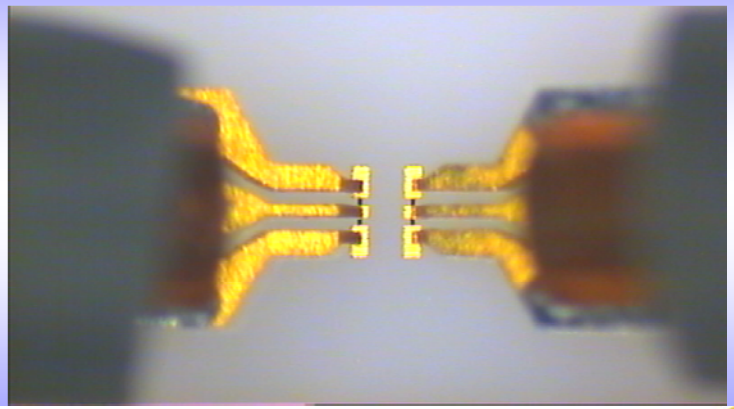


Alignment Marks: Probes Just Touching ISS

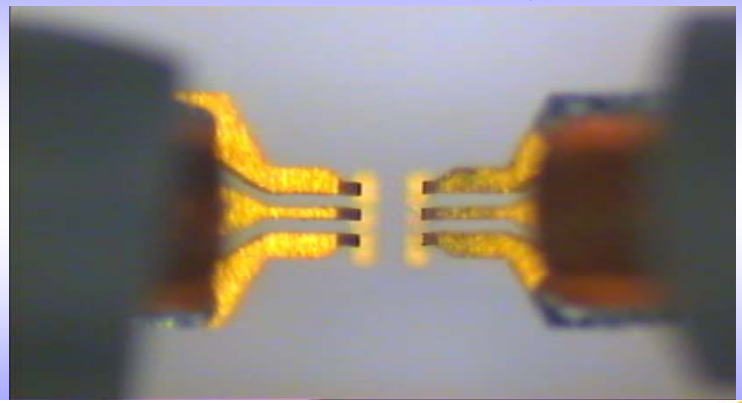


- Standards are located either on-wafer or on an impedance standard substrate (ISS)
- On-wafer standards is by far the best choice, because the probe-to-wafer interface can be electromagnetically the same for calibration, verification and all subsequent measurements
- Ideally, the reference planes within the on-wafer standards should have the same line geometries as those on the chip
- With a precision ISS, the standards can be fabricated to much tighter tolerances, using laser-trimming (to achieve an almost exact value of 50 Ω at DC only) and made traceable
- If a calibration is performed using a 635 μm thick alumina ISS and the verification is performed using 200 μm thick GaAs on-wafer standards then errors occur at mm-waves
- For this reason, the NPL (UK) and the NIST (US) have developed GaAs ISS wafers with calibration standards and verification components of certified quality

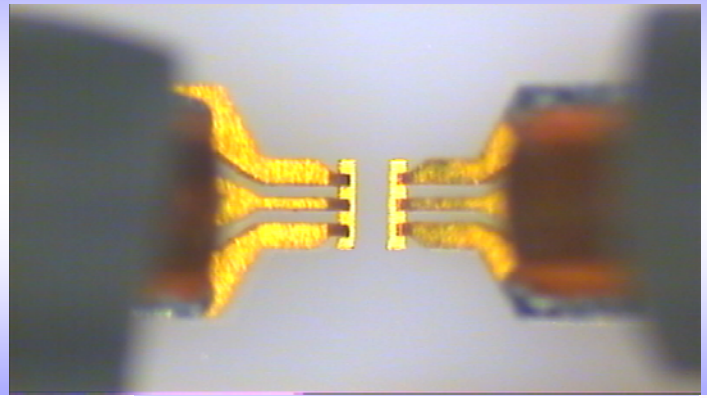
50 Ω LOAD Standard



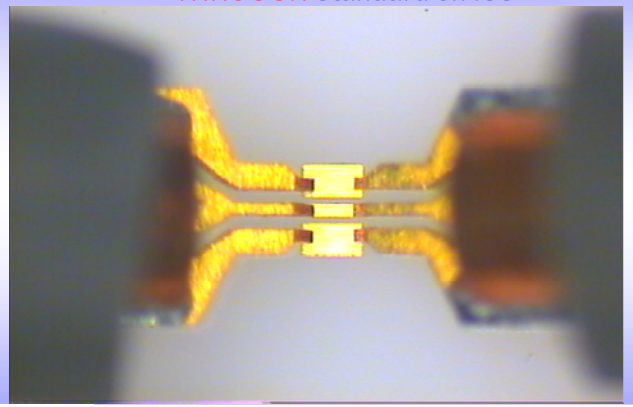
OPEN Standard: Probes Up



SHORT Standard: Probes Down



THROUGH Standard on ISS



LRM calibration

- line-reflect-match (LRM) calibration is preferred to TRL
- the multiple CPW delay lines required with the TRL calibration are effectively replaced by the CPW 50 Ω load, to theoretically represent an infinitely long delay line
- this results in the following advantages:

– an ultra-wideband calibration can be achieved (e.g. from DC to 120 GHz)
– the probes can be set in a fixed position
– automatic calibration routines can be applied
– reflections and unwanted modes in long CPW delay lines are avoided
– a considerable saving of wafer/ISS area can be made

- For the ultimate in ultra-wideband measurement accuracy, there is strong support for having TRL calibration above 1 GHz combined with LRM below 1 GHz
  - the LRM standards should be characterised at DC and at 1 GHz (using TRL); conventional modelling techniques can be used to interpolate the results
- A 2-port probe station traditionally uses a 12-term error model, although a 16-term error model has been introduced that requires 5 calibration standards
  - this more accurate model can correct for poor grounding and the additional leakage paths and coupling effects encountered with open-air probing

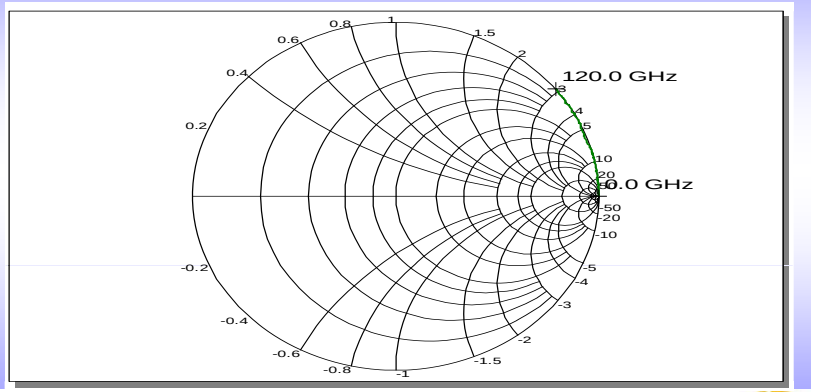
LRRM calibration

- with SOLT and LRM, the accuracy to which the load is known directly determines the accuracy of the measurements
- loads inevitably have some parasitic shunt capacitance (which is equivalent to having negative series inductance)
- loads have frequency-dependent resistance due to ‘skin effect’
- with microstrip, there will be significant series inductance associated with the short and load standards
- LRRM calibration is a more accurate version of the standard LRM calibration, in which load-inductance correction is incorporated by including an extra reflection standard. Unlike SOLT, the OPEN is not a critical standard with LRRM.

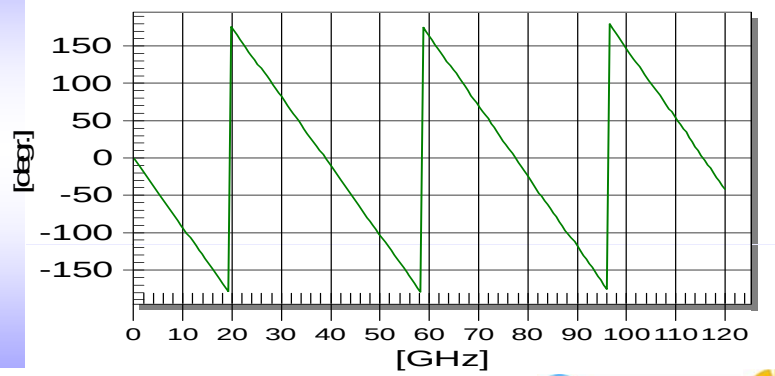
	Z_0 Reference	Inherently Consistent	Probe Card Support	Absolute Accuracy
SOLT	Trimmed Resistor	No	Fair	Fair
TRL	Transmission Lines	Yes	Poor	Best (if Corrected)
LRM/ LRRM	Trimmed Resistor	Yes	Fair	Good
SOLR	Trimmed Resistor	Yes	Best	Good

- SOLT: open standard not good enough above 50 GHz
- LRM: convenient, but not very repeatable
- LRRM: less sensitive to probe placement errors
- TRL/LRL: difficult to get good results but widely considered the best

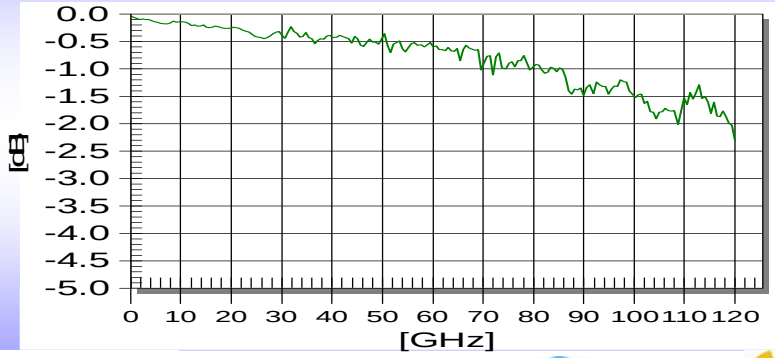
Verification and Measurements: S11 of OPEN Verification



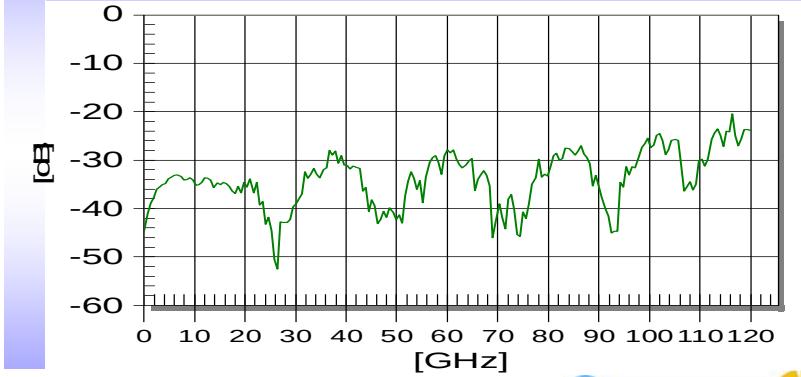
S21 Phase of ISS 25 ps THROUGH Verification



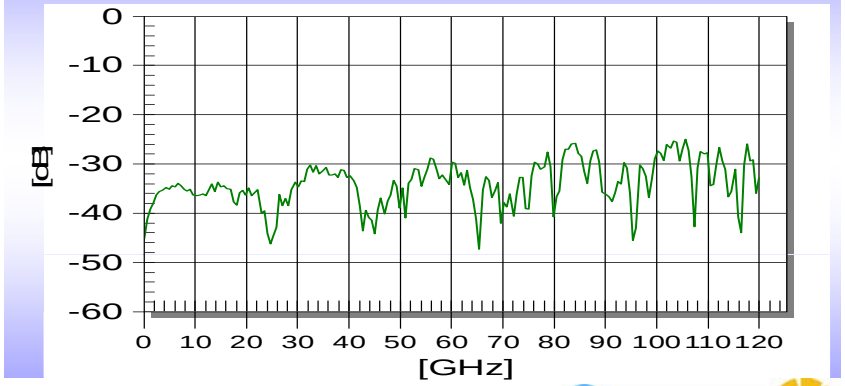
S21 Magnitude of ISS 25 ps THROUGH Verification



S11 Magnitude of ISS 25 ps THROUGH Verification



S22 Magnitude of ISS 25 ps THROUGH Verification



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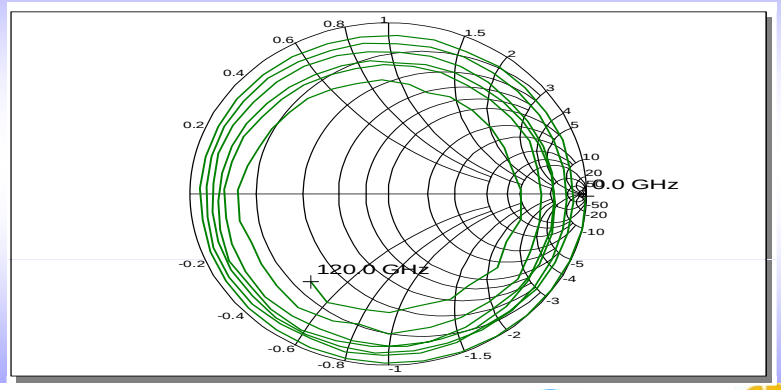
Radio Frequency Engineering
Lecture #4 S-Parameter Analysis

ISS 25 ps CPW Line: S11 Reflect Verification



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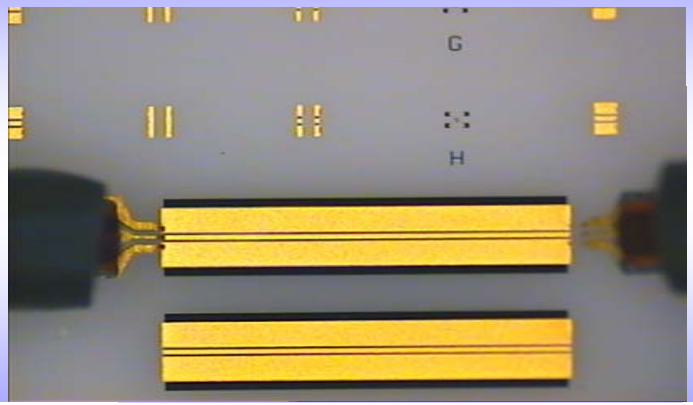
Radio Frequency Engineering
Lecture #4 S-Parameter Analysis

ISS 25 ps CPW Line Reflection Verification



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Radio Frequency Engineering
Lecture #4 S-Parameter Analysis

Measurement Errors

- Even when the system has been successfully calibrated, measurement errors (or uncertainty) can still occur. Some of the more common sources of errors are as follows:

  - probe placement errors
  - temperature variation between calibration and measurement
  - cable-shift induced phase errors between calibration and measurement
  - radiation impedance changes due to the probes/wafer chuck moving
  - matrix renormalisation not being performed with multiple port MMICs
  - resonant coupling of the probes into adjacent structures
  - low frequency changes in the characteristic impedance and effective permittivity of both microstrip and CPW lines
  - optically-induced measurement anomalies associated with voltage-tunable analogue-controlled MMICs

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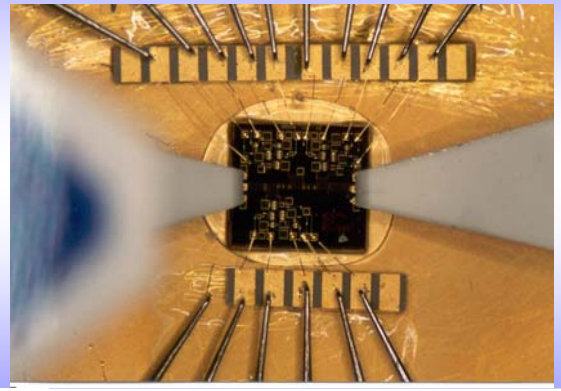
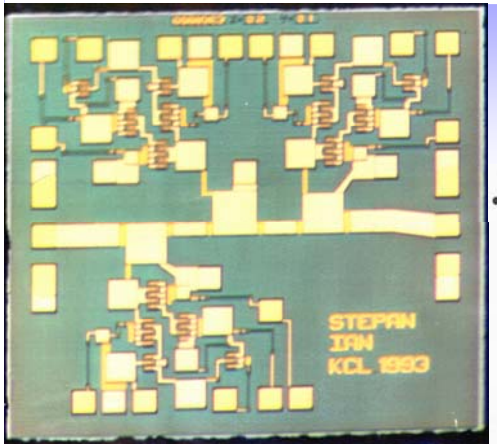
Applying DC Bias

- Depending on the nature and complexity of the device or circuit under test, DC bias can be applied to an MMIC in a number of ways:
  - through the RF probes, via bias-tees in the VNA's test set
  - through single DC needles, mounted on probe station positioners
  - with multiple DC needle probe card, which may be mounted on a positioner
- The DC probe needle has significant inductance, and as a result, provides RF de-coupling for the bias lines that helps to prevent stability problems
- Additional off-chip de-coupling capacitors and resistors can usually be added to the card to further minimise the risk of unwanted oscillations
- With multiple DC needle probe card, standard in-house DC footprints enable card re-use

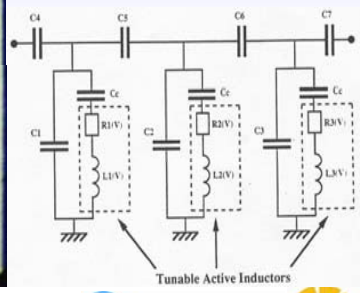
- This low-cost solution has a number of advantages for use in the R&D laboratory:
  - the high inductance bond wires and 100 pF off-chip de-coupling capacitors minimise the risk of unwanted oscillations
  - when designing the MMIC layout, the DC probe pads do not need to be arranged in a linear array along the edges of the chip. This provides greater design layout flexibility
  - the linear array of off-chip capacitors automatically provides a standard in-house DC footprint, reducing long-term measurement costs considerably
  - the probeable area of the off-chip capacitors is approximately 15 times larger than that of the MMIC probe pads and the capacitors can withstand greater mechanical forces
  - in-house DC probe cards can be made by hand, because of the relaxation in manufacturing precision, reducing short-term costs considerably

Low-Cost DC Biasing of MMIC Prototypes

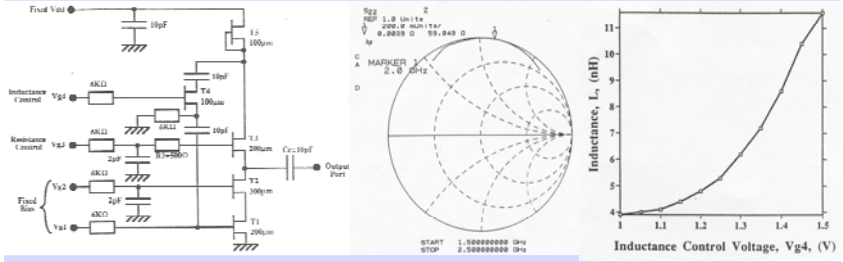




2 GHz MMIC band-pass filter (employing 3 active inductors)



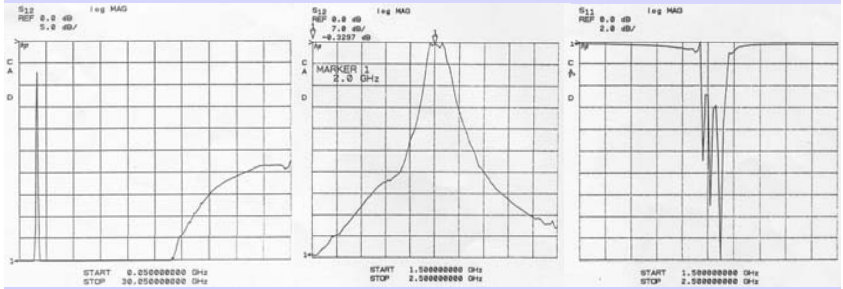
'all-transistor' active inductors (equivalent Q-factor of 15,000)



Time-domain Gating

- VNAs can be upgraded with a synthetic-pulse time-domain reflectometry (TDR) option
- The discrete form of the inverse Fourier transform (IFT) is applied to a real sequence of harmonically related frequency-domain (F-D) measurements
- This is directly equivalent to mathematically generating synthetic unity-amplitude impulses (or steps), which are then 'applied' to the embedded MMIC
- The resulting time-domain (T-D) reflection and transmission responses can then be analysed to provide information about the MMIC and test fixture discontinuities
- In reflection measurements, it is possible to remove the effects of unwanted impedance mismatches or else isolate and view the response of an individual feature
- With a multiple port test-fixture, transmission measurements can give the propagation delay and insertion loss of signals travelling through a particular path by removing the responses from the unwanted paths

2 GHz MMIC active band-pass filter frequency performance



- With an MMIC fed with transmission lines that only support a pure TEM mode of propagation, time and actual physical distance are simply related:

$$\textit{Physical Distance} = \begin{cases} c\,\Delta t\,\zeta/2 & \text{with reflection measurements} \\ c\,\Delta t\,\zeta & \text{with transmission measurements} \end{cases}$$

where,

c = speed of light in free space

Δt = time difference, relative to a reference (e.g. $t = 0$)

$$\zeta = \frac{1}{\sqrt{\varepsilon_r}} = \text{velocity factor}$$

Also, frequency-domain nulls in $|S_{11}|$ are at frequency harmonics of $\dfrac{1}{\Delta t}$

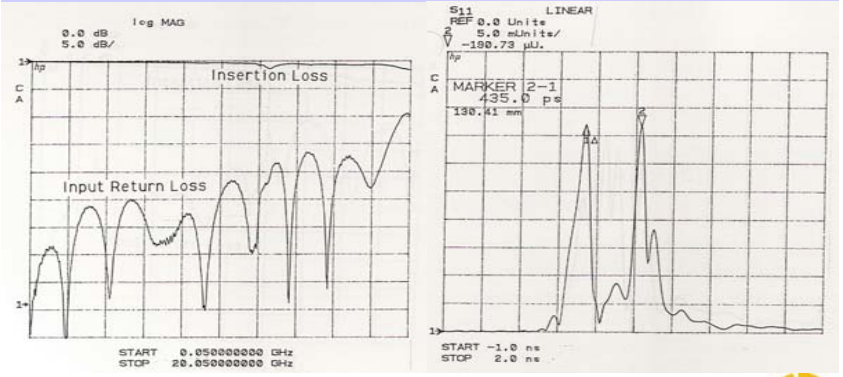
where, Δt = time difference, between two reflected impulses

- If the feed lines are non-TEM, and therefore dispersive, impulse spreading will occur, which could significantly distort the impulse shape (in time and amplitude)

✍ De-embedding using synthetics-pulse TDR is not de-embedding in the true sense
✍ It is specifically T-D gating, which can isolate a time feature and emphasise its frequency response
✍ With time-gating, a mathematical window (called a gate or time filter) is used to isolate the embedded DUT, so that only the DUT's frequency response can be emphasised
✍ When the gate is on, all reflections outside the gate are set to zero. This is equivalent to terminating the DUT with the complex conjugate of its respective port impedance(s)
✍ The synthetic-pulse TDR option can be a very useful tool, although it can suffer from a number of sources of errors:

- Noise Errors
- Frequency-Domain Window Errors
- Discontinuity Errors
- Time-Domain Window Errors

50 Ω microstrip through-line: (a) frequency-domain power responses and (b) corresponding time-domain response for input voltage reflection coefficient



✍ 2.9 mm GaAs MMIC 55 Ω through-line at the centre of a 25.4 mm alumina chip carrier:

- VNA was calibrated with a 20 GHz bandwidth and 401 frequency points
- this combination provides a minimum response resolution and maximum range values of 60 ps and 20 ns, respectively
- in the T-D response of the input port's voltage reflection coefficient:
  - first and last peaks correspond to the impedance mismatches associated with the coaxial-to-microstrip transitions of the input and output ports, respectively
  - two centre peaks are reflections associated with the microstrip-to-MMIC transitions
- accurate de-embedding would not be possible using T-D gating. This is because the unwanted reflections cannot be resolved down to the baseline
- if de-embedding were attempted in the above example then the ripples in the F-D responses would be smoothed out, but this is NOT accurate de-embedding
- in order to achieve accurate de-embedded measurements, a VNA with more bandwidth, or alternatively, a real-pulse TDR system having ultra-short impulses, can be used

Embedded 55 Ω MMIC through-line: (a) frequency-domain power responses and (b) corresponding time-domain response for input voltage reflection coefficient